

Low-Power Digital Microwave Radiometer Technologies

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Abstract - Synthetic-Thinned Aperture Radiometers (STARs), will be used in low-Earth and geostationary orbits for future Earth Science measurements. The detector stages of STAR sensors, and other digital microwave radiometers, are typically based on digital cross- and self-correlators. For practical implementation, digitizing microwave receivers, analog-to-digital converters (ADCs), and digital correlators of minimal mass, power, and volume are required. We have demonstrated an ultra-low power (ULP) 0.5V CMOS cross-correlator that dissipates 1mW/correlation. A 625-baseline (25 inputs) cross-correlator has been fabricated in ULP CMOS (CULPRT) and is currently under test. Digitizing receivers have been fabricated using a combination of InP and GaAs MMICs at 11, 18, and 37 GHz with a worst-case power dissipation of 1.5W per receiver. Finally, custom ADCs are under development in both CULPRT CMOS and SiGe. The CULPRT ADC has been fabricated and tested demonstrating a minimum of 125 MS/s with 2-bit quantization. A prototype 2-bit SiGe ADC has been fabricated and demonstrated 500-MHz sampling rate with 2-GHz input bandwidth. The combination of low-power microwave receivers, ADCs, and digital correlator will enable Earth science measurements envisioned in the future.

I. INTRODUCTION

A diverse group of communities, including land surface hydrology and atmospheric science, within the NASA Earth Science Enterprise are focused on achieving passive microwave remote sensing measurements with spatial resolutions finer than can be achieved by current radiometer systems. The problem becomes especially difficult with the oversubscription of spacecraft resources when larger antenna apertures are required to satisfy smaller footprints for low-Earth and geostationary orbits. Next generation radiometer systems are now being proposed using Synthetic-Thinned Aperture Radiometer (STAR) technology [1] that promises higher spatial resolution than comparably sized mechanical scanners as well as antenna software-based antenna beam-forming to match the geometry and size of other sensors' footprints. Advanced low-power/flight qualified digital correlator and ADC Application Specific Integrated Circuits (ASICs) have been produced, under several ESTO IIP and ACT programs, for use in spaceborne STARs. These technologies have already

been earmarked for use in future large-aperture spaceborne radiometer concepts.

II. ANALOG-TO-DIGITAL CONVERTERS

A. Ultra-low Power CMOS ADC

The Center for Advanced Microelectronics And Microbiology Research (CAMBR) at the University of Idaho has fabricated custom ASICs, under the Lightweight Rainfall Radiometer (LRR) IIP, that will significantly enhance the performance while simultaneously reducing the power required by a spaceborne STAR sensor. An analog-to-digital converter (ADC) has been fabricated to match the capabilities of a correlating radiometer. Figure 1 shows the ADC and digital correlator chipset that are the key digital signal processing units of the proposed STAR sensor.

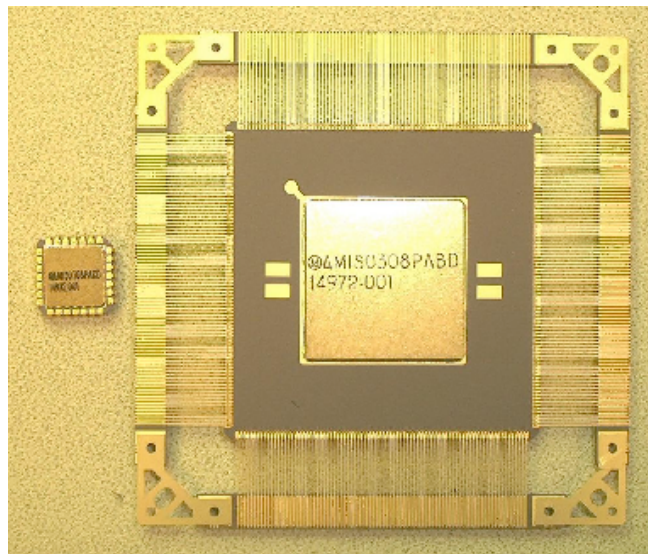


Figure 1 - CULPRT Digital Correlator and ADC chip pair

This ADC has four quantization levels (2-bits) that have adjustable boundaries (input voltage thresholds). These thresholds are individually set by high precision digital-to-analog converters embedded within the ADC itself and are externally controlled by the user. The ADC has been tested and it meets the requirements of 30 mW of power at a clock rate of 84 MHz for

the next generation LRR receiver that will be delivered to GSFC on May 2003. The ADC embedded in the next generation LRR receiver is shown in Figure 2. The ADC's Power requirement increases to 100 milliwatts as the clock rate is increased to the 224 MHz rate that is required for a future 37 GHz spaceborne STAR sensor. The bandwidth of the analog input stage of the ADC is significantly higher than the allowed clock rate. This permits the ADC to operate in a sub-sampling mode, as required by the current STAR sensor design.

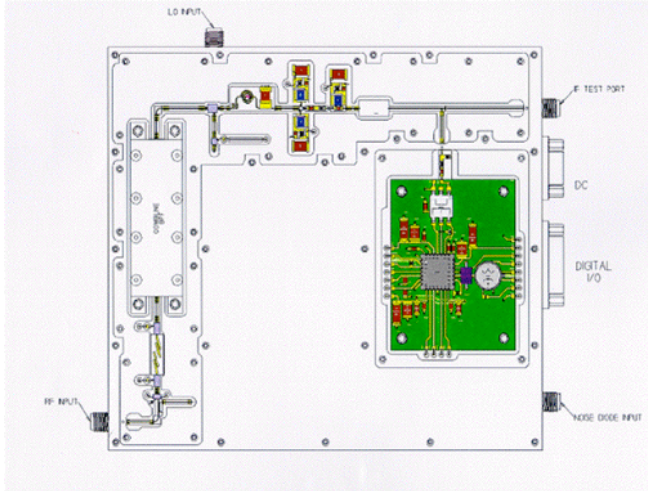


Figure 2 - CULPRT ADC in the Next Generation LRR (NGLRR) MMIC receiver unit

B. Direct Sampling SiGe ADC

A low-power Silicon Germanium (SiGe) ADC is being developed by NASA GSFC and the Center for Advanced Microwave Research and Applications (CAMRA) at Morgan State University under an ACT project [3]. A prototype two-bit ADC has been demonstrated in 0.8 μ m

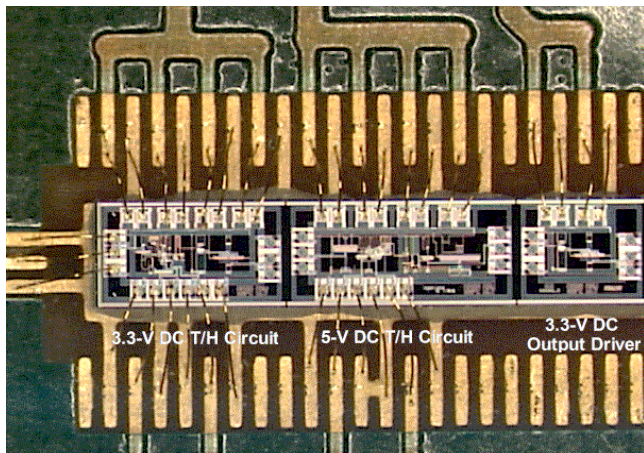


Figure 3. Photograph of SiGe ADC die.

SiGe-BiCMOS permits 500-MHz sampling rate with a 2 GHz input bandwidth. It dissipates 220 mW with a 3.3V

supply. The ADC requirements have been set to allow the chip to be used in an L-band STAR for soil moisture remote sensing. The ADC uses a diode-bridge based track-and-hold amplifier to allow it to operate in undersampling mode (see Fig.3). The quantizer is a four-level (three-comparator) flash architecture and uses current-mode logic (CML) for the thermometer-to-binary decoder. The CML power dissipation is independent of sampling rate, but can be optimized for a maximum operating rate. Currently the design is being optimized for minimum power dissipation and implementation in a domestic 0.35 μ m SiGe BiCMOS process. Power dissipation is expected to decrease because of the higher transition frequency in the smaller feature size process.

III. DIGITAL CORRELATORS

Digital correlators are a key hardware component of the new STAR radiometer designs. Combinations of antenna signals are correlated and the resulting spatial coefficients are processed by image reconstruction algorithms. The following digital correlator chip designs were developed using the CMOS Ultra-Low Power Radiation Tolerant (CULPRT) process at the Center for Advanced Microelectronics and Biomolecular Research (CAMBR) of the University of Idaho.

A. Single-Channel Correlator

A single-channel cross-correlator was developed under an ATIP project for microwave polarimetry to demonstrate the low power dissipation of CULPRT for correlator applications [4]. The correlator is a single-baseline (i.e. two complex input) cross-correlator with inputs for three-level quantized in- and quadrature-phase signals. The maximum clock rate is 500 MHz. Because the signals are quantized using only three levels, the multipliers only produce outputs equaling -1, 0, or +1. The chip contains accumulators for the +1 and -1 quantization bins of the individual inputs for total power measurement. For cross-correlation measurement, all possible product combinations between signals are accumulated in positive and negative accumulators. The core logic is implemented using 0.5-V CULPRT and the microprocessor interface using 3.3-V CMOS. The chip has been operated in the laboratory and power dissipation was measured for varying clock rates. Power dissipation of 1 mW at 100 MHz and 2 mW at 500 MHz clock was demonstrated.

B. 625-baseline Correlator

The design and fabrication of a 25x25 input (625 cell) digital correlator chip were developed as part of the Lightweight Rainfall Radiometer (LRR) Instrument Incubator Program (IIP). The correlator and the 2-bit ADC CULPRT 0.5V chipset have already been shown in Fig. 1. The chip is designed with a radiation tolerant architecture, dissipating 1.5W (DC) at 224 MHz, making it TRL-4 ready for use in STAR spaceborne prototypes. This device performs complex cross correlations of all pairs of digitized input signals, as well as computing total power self-correlations of each individual signal. The chip is capable of handling up to 25 input channels at clock rates up to 224 MHz (as

required for a spaceborne STAR design at 37 GHz). The chip also includes individual “totalizer” counters for each quantization bin of every input channel that generates real-time histograms of the distribution of signal strength across the ADC input voltage ranges. This information is needed to produce the STAR brightness temperature images with a maximum signal-to-noise ratio without resorting to very high precision ADC and correlator subsystems. The ability to perform all necessary digital signal processing using only 2-bit precision is needed in order to keep the power requirements of the system low. Large array radiometers, such as for soil moisture measurement, will need significantly more channels. The 625 cell correlator chip is a scalable design that can be tied together to correlate large numbers of channels. Fig. 2 illustrates an architecture of 100 input channels that requires 31 correlator chips.

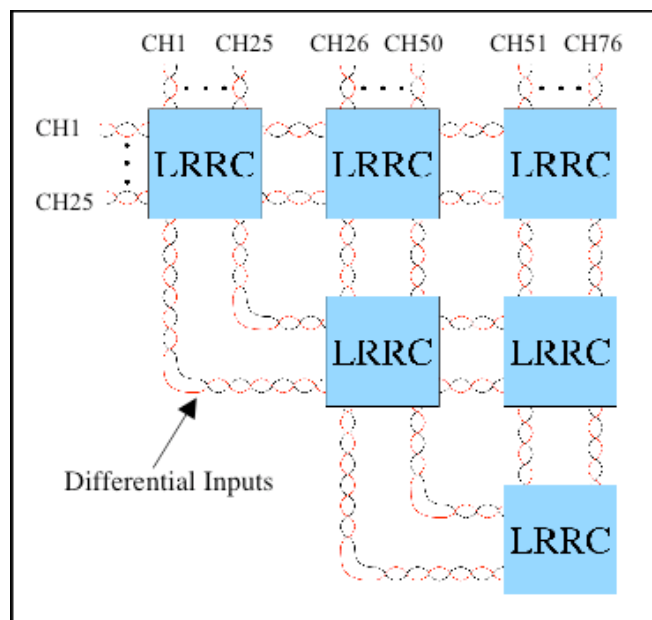


Figure 3 – A total of 10 CULPRT digital correlator chips are required for a 100 x 100 sensor channel architecture (partial view of matrix)

IV. SUMMARY

Several developments in the area of low-power digital microwave radiometer technologies for STAR have been presented. Notably, custom correlator ICs with companion ADCs are being developed to address the need for low power dissipation and space flight readiness.

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